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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,518	12/31/2003	Kenneth D. Poulton	10021119-1	9241

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,518	POULTON ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/31/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 as originally filed are pending in the instant application. Of these, there are 2 independent claims and 20 dependent claims.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 19-22** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The term "*electrically proximate*" in **claims 1 and 13** is a relative term which renders the claim indefinite. The term "*electrically proximate*" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For the purpose of this Office action, the Examiner interprets said limitation as "*electrically connected*".

6. **Claims 2-12 and 14-22** are rejected due to their dependence on claims 1 and 13 respectively.

7. **Claim 2** recites the limitation "*the digital data words*" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 1 refers to a "*digital data word*" in line 4.

8. **Claim 19** recites the limitation "*the circuit*" in line 4. There is insufficient antecedent basis for this limitation in the claim. Claim 13 refers to a "*mixed-signal circuit*" in line 1 and "*an analog circuit*" in line 2. For the purpose of this Office action, the Examiner interprets the limitation "*the circuit*" as "*the mixed-signal circuit*"

9. **Claims 20 and 21** are rejected due to their dependence on claim 19.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. **Claims 1-6, 8-17, and 22** are rejected under 35 U.S.C. 102(b) as being anticipated by Corry et al. (US 5,649,160).

12. **Claim 1** Is taught by Corry as:

a. *A method for reducing variations in noise and temperature in a mixed-signal circuit.* Abstract lines 1-3.

b. *The method comprising: providing memory electrically proximate an analog circuit.* Column 3 lines 11-19.

c. *Receiving a digital data word at the memory.* Column 4 lines 27-35 shows that data packets consisting of eight bytes of information are sent on a ring to router 27 of figure 1. Column 5 lines 21-22 shows that the router 27 contains memory 29.

d. *Determining whether the data word is a desired data word.* Column 6 lines 21-24 shows that each packet contains a valid bit indicating whether or not the packet is valid.

e. *Performing a dummy write to the memory when the data word is not a desired data word.* Column 6 lines 60-66 show that if the valid bit is not asserted, the address selected is zero. Column 6 lines 34-37 show that address zero is reserved as a dummy location.

f. *And writing the data word to the memory when the data word is a desired data word.* Column 6 line 66 to column 7 line 2 shows that when R/W is asserted, the packet's address is loaded as the write address so as to perform an actual write.

13. **Claim 2** is taught by Corry as:

g. *The method of claim 1, in which: the receiving comprises processing an analog input signal and generating the digital data words.* Column 4 lines 41-46

show that an I/O device receives an analog signal and converts it to a digital format.

14. **Claim 3** is taught by Corry as:

h. *The method of claim 1, in which: the memory comprises dummy memory and acquisition memory.* Column 6 lines 36-39 show that address zero is reserved as a dummy location, the remainder of the memory where valid writes are stored may be considered acquisition memory.

i. *The performing comprises performing the dummy write to the dummy memory.* Column 6 lines 36-39 show that address zero is reserved as a dummy location, and that when a dummy write to address zero is performed no valid data is overwritten.

j. *And the writing comprises writing the data word to the acquisition memory.* Column 6 line 66 to column 7 line 2 shows that when R/W is asserted, the packet's address is loaded as the write address so as to perform an actual write to the selected memory location.

15. **Claim 4** is taught by Corry as:

k. *The method of claim 1, in which: the determining comprises: providing an enable signal having a dummy value and an acquisition value.* Column 6 lines 21-24 shows that each packet includes a valid bit indicating whether or not the packet is valid.

l. *And determining whether the enable signal is at the dummy value or the acquisition value*. Column 6 lines 63-66 show that if the valid bit is not asserted, the address loaded is zero.

m. *The performing comprises performing the dummy write to the memory when the enable signal is at the dummy value*. Column 6 lines 36-39 shows that when the address zero is loaded because the valid bit is not asserted, a dummy write is performed.

n. *And the writing comprises writing the data word to the memory when the enable signal is at the acquisition value*. Column 6 line 66 to column 7 line 2 shows that when R/W is asserted and the valid bit is asserted, the packet's address is loaded as the write address so as to perform an actual write.

16. **Claim 5** is taught by Corry as:

o. *The method of claim 4, in which: the memory comprises dummy memory and acquisition memory*. Column 6 lines 36-39 show that address zero is reserved as a dummy location, the remainder of the memory where valid writes are stored may be considered acquisition memory.

p. *The performing comprises performing the dummy write to the dummy memory*. Column 6 lines 36-39 show that address zero is reserved as a dummy location, and that when a dummy write to address zero is performed no valid data is overwritten.

q. *And the writing comprises writing the data word to the acquisition memory.* Column 6 line 66 to column 7 line 2 shows that when R/W is asserted, the packet's address is loaded as the write address so as to perform an actual write to the selected memory location.

17. **Claim 6** is taught by Corry as:

r. *The method of claim 5, in which the dummy memory comprises no more than a single memory location in the memory.* Column 6 lines 36-39 show that address zero is reserved as a dummy location.

18. **Claim 8** is taught by Corry as:

s. *The method of claim 1, in which: the memory comprises memory locations corresponding to memory addresses.* Column 6 lines 27-37 show that addresses are applied to either the read port of the memory or the write port of the memory, and that address zero is reserved as a dummy location. Accordingly, memory locations correspond to memory addresses.

t. *And the method additionally comprises initializing a memory address.* Column 4 line 66 to column 5 line 3 show that in a memory transaction, bit lines within the memory are precharged, which shows an initialization of the memory.

u. *The performing comprises performing the dummy write to the memory location indicated by the memory address.* Column 6 lines 36-39 show that

address zero is reserved as a dummy location, and that when a dummy write to address zero is performed no valid data is overwritten.

v. *And the writing comprises writing the data word to the memory location indicated by the memory address.* Column 6 line 66 to column 7 line 2 shows that when R/W is asserted and the valid bit is asserted, the packet's address is loaded as the write address so as to perform an actual write.

19. **Claim 9** is taught by Corry as:

w. *The method of claim 8, in which the performing additionally comprises maintaining the same memory address after the dummy write has been performed.* Column 6 lines 27-34 shows that the address is stored in the multiplexer for four clock cycles, the time required to perform the write, and a new address is then loaded for the next write. If the next read is not a valid write, the dummy address of zero would be maintained.

20. **Claim 10** is taught by Corry as:

x. *The method of claim 8, in which the writing additionally comprises changing the memory address after the data word has been written.* Column 6 lines 27-34 shows that a new address is selected every four clock cycles. In order to write to a different memory location, the memory address must be changed at some point after the data word has been written.

21. **Claim 11** is taught by Corry as:

y. *The method of claim 8, in which the dummy write comprises writing a dummy data word to the memory location indicated by the memory address.* Column 6 lines 36-39 show that a dummy write to address zero is performed. The cited section states that when a dummy write to address zero is performed no valid no valid data is overwritten. The only way overwriting valid data would be a possibility is if the dummy data is actually written to the memory.

22. **Claim 12** is taught by Corry as:

z. *The method of claim 8, in which the dummy write comprises writing the data word that is not a desired data word to the memory location indicated by the memory address.* Column 6 lines 36-39 show that a dummy write to address zero is performed. The cited section states that when a dummy write to address zero is performed no valid no valid data is overwritten. The only way overwriting valid data would be a possibility is if the dummy data is actually written to the memory.

23. **Claim 13** is taught by Corry as:

aa. *A mixed-signal circuit, comprising: an analog circuit.* I/O devices 25 of figure 1 are shown in figure 2 to contain an analog front end 35.

bb. *Memory electrically proximate to the analog circuit, the memory connected to receive digital data words.* Item 29 of figure 5 is shown to receive data through data in pipeline 70, column 4 lines 28-35 show that the data is digital.

cc. *And a memory controller connected to the memory.* Column 5 lines 42-43 shows that packet router 27 controls access to the shared memory.

dd. *The memory controller operable to cause the memory to write to the memory each of the data words that is a desired data word.* Column 6 line 66 to column 7 line 2 shows that when R/W is asserted, the packet's address is loaded as the write address so as to perform an actual write.

ee. *And additionally to perform a dummy write to memory for each of the data words that is not a desired data word.* Column 6 lines 60-66 show that if the valid bit is not asserted, the address selected is zero. Column 6 lines 34-37 show that address zero is reserved as a dummy location.

24. **Claim 14** is taught by Corry as:

ff. *The circuit of claim 13, additionally comprising an analog/digital circuit operable to process an analog input signal and to generate the digital data words.* Column 4 lines 41-46 shows that I/O devices 25 use an A/D converter to sample an analog output signal and produce digital data.

25. **Claim 15** is taught by Corry as:

gg. *The circuit of claim 14, in which the analog/digital circuit comprises an analog-to-digital converter.* Column 4 lines 41-46 shows that I/O devices 25 use an A/D converter to sample an analog output signal and produce digital data.

26. **Claim 16** is taught by Corry as:

hh. *The circuit of claim 13, in which: the memory controller is responsive to an enable signal and generates an address signal.* Column 6 lines 21-24 shows that each packet includes a valid bit indicating whether or not the packet is valid. Column 6 line 60 to column 7 line2 shows that the packet router generates a new address for the next memory reference and load it into one of the address mux-flops 87 and 89 depending on whether the access is a write or a read.

ii. *The enable signal has a dummy value when the data word is not a desired data word and an acquisition value when the data word is a desired data word.* The valid bit is shown in column 6 lines 21-24 to show whether or not the packet is valid.

jj. *The memory comprises dummy memory and acquisition memory, and stores the data word where designated by the address signal.* Column 6 lines 36-39 shows that address zero is reserved as a dummy location, which makes the rest of the memory acquisition memory. Column 6 line 60 to column 7 line 2 shows that the data is written to address zero if the packet is not valid and to the address designated by the packet if the packet is valid.

kk. *And the memory controller provides the address signal corresponding to the dummy memory when the enable signal is at the dummy value and provides the address signal corresponding to the acquisition memory when the enable signal is at the acquisition value.* Column 6 line 60 to column 7 line 2 shows that the data is written to address zero if the valid bit is not asserted and to the address designated by the packet if the packet is valid.

27. **Claim 17** is taught by Corry as:

ll. *The circuit of claim 16, in which the dummy memory comprises a single memory location in the memory.* Column 6 lines 36-39 show that address zero is reserved as a dummy location.

28. **Claim 22** is taught by Corry as:

mm. *The circuit of claim 13, in which: the memory controller generates an address signal.* Column 6 line 60 to column 7 line2 shows that the packet router generates a new address for the next memory reference and load it into one of the address mux-flops 87 and 89 depending on whether the access is a write or a read.

nn. *The memory stores the data word where designated by the address signal in each clock cycle.* Column 6 lines 27-34 shows that the data is written to either an address previously stored in an address register or a new address stored in an address register

oo. *And the memory controller is operable to maintain the address signal for a given number of clock cycles and changes the address signal after the given number of clock cycles.* Column 6 lines 32-34 shows that a new address is selected every four clock cycles, and the previous address is selected during the intervening three clock cycles.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. **Claims 7 and 18** rejected under 35 U.S.C. 103(a) as being unpatentable over Corry et al. (cited *supra*).

31. **Claim 7** is taught by Corry as shown *supra* with respect to claim 5.

32. Corry does not disclose expressly the dummy memory comprising a range of addresses.

33. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have allowed multiple dummy memory addresses, thereby providing a range of dummy memory addresses in the memory of Corry.

34. The motivation for doing so is provided by *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), which held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.

35. Therefore it would have been obvious to modify the memory of Corry to include a range of dummy memory locations in the memory to obtain the invention as specified in claim 7.

36. **Claim 18** is taught by Corry as shown *supra* with respect to claim 16.

37. Corry does not disclose expressly the dummy memory comprising a range of addresses.

38. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have allowed multiple dummy memory addresses, thereby providing a range of dummy memory addresses in the memory of Corry.

39. The motivation for doing so is provided by *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), which held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.

40. Therefore it would have been obvious to modify the memory of Corry to include a range of dummy memory locations in the memory to obtain the invention as specified in claim 18.

Allowable Subject Matter

41. **Claims 19-21** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

42. **Claim 19** recites the limitation "*the memory controller is responsive to a decimation ratio signal and generates an address signal*; *the circuit additionally comprises a decimator operable in response to the decimation ratio signal to generate output data words in response to the data words*, *the output data words comprising, in a given number of clock cycles, respective dummy data words and a desired data word*". This limitation, supported by the specification at least at page 11 lines 15-30, is not taught or suggested by the prior art of record.

43. **Claims 20 and 21** depend from claim 19 and would be allowable for at least the reasons cited with respect to claim 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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